FDS4465
P-Channel 1.8V Specified PowerTrench® MOSFET

General Description
This P-Channel 1.8V specified MOSFET is a rugged gate version of Fairchild Semiconductor’s advanced PowerTrench process. It has been optimized for power management applications with a wide range of gate drive voltage (1.8V – 8V).

Applications
• Power management
• Load switch
• Battery protection

Features
• −13.5 A, −20 V.  \( R_{DS(ON)} = 8.5 \, m\Omega \) @ \( V_{GS} = -4.5 \, V \)
  \( R_{DS(ON)} = 10.5 \, m\Omega \) @ \( V_{GS} = -2.5 \, V \)
  \( R_{DS(ON)} = 14 \, m\Omega \) @ \( V_{GS} = -1.8 \, V \)
• Fast switching speed
• High performance trench technology for extremely low \( R_{DS(ON)} \)
• High current and power handling capability

Absolute Maximum Ratings  \( T_{A}=25^\circ C \) unless otherwise noted

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Ratings</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{DS} )</td>
<td>Drain-Source Voltage</td>
<td>−20</td>
<td>V</td>
</tr>
<tr>
<td>( V_{GS} )</td>
<td>Gate-Source Voltage</td>
<td>±8</td>
<td>V</td>
</tr>
<tr>
<td>( I_D )</td>
<td>Drain Current – Continuous</td>
<td>−13.5</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>– Pulsed</td>
<td>−50</td>
<td></td>
</tr>
<tr>
<td>( P_D )</td>
<td>Power Dissipation for Single Operation</td>
<td>(Note 1a)</td>
<td>2.5</td>
</tr>
<tr>
<td></td>
<td>(Note 1b)</td>
<td>1.5</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(Note 1c)</td>
<td>1.2</td>
<td></td>
</tr>
<tr>
<td>( T_J, T_{STG} )</td>
<td>Operating and Storage Junction Temperature Range</td>
<td>−55 to +175</td>
<td>°C</td>
</tr>
</tbody>
</table>

Thermal Characteristics
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Ratings</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{JA} )</td>
<td>Thermal Resistance, Junction-to-Ambient (Note 1a)</td>
<td>50</td>
<td>°C/W</td>
</tr>
<tr>
<td>( R_{JC} )</td>
<td>Thermal Resistance, Junction-to-Case (Note 1)</td>
<td>25</td>
<td>°C/W</td>
</tr>
<tr>
<td>( R_{JA} )</td>
<td>Thermal Resistance, Junction-to-Ambient (Note 1c)</td>
<td>125</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

Package Marking and Ordering Information

<table>
<thead>
<tr>
<th>Device Marking</th>
<th>Device</th>
<th>Reel Size</th>
<th>Tape width</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>FDS4465</td>
<td>FDS4465</td>
<td>13”</td>
<td>12mm</td>
<td>2500 units</td>
</tr>
</tbody>
</table>
## Electrical Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Off Characteristics</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BV_{DSS}</td>
<td>Drain–Source Breakdown Voltage</td>
<td>V_{GS} = 0 V, I_{D} = –250 μA</td>
<td>–20</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>∆B_{DSS}</td>
<td>Breakdown Voltage Temperature Coefficient</td>
<td>I_{D} = –250 μA, Referenced to 25°C</td>
<td>–12</td>
<td></td>
<td></td>
<td>mV/°C</td>
</tr>
<tr>
<td>I_{DSS}</td>
<td>Zero Gate Voltage Drain Current</td>
<td>V_{DS} = –16 V, V_{GS} = 0 V</td>
<td>–1</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>I_{GSF}</td>
<td>Gate–Body Leakage, Forward</td>
<td>V_{GS} = 8 V, V_{DS} = 0 V</td>
<td>100</td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>I_{GSR}</td>
<td>Gate–Body Leakage, Reverse</td>
<td>V_{GS} = –8 V, V_{DS} = 0 V</td>
<td>–100</td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>On Characteristics (Note 2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{GS(th)}</td>
<td>Gate Threshold Voltage</td>
<td>V_{DS} = V_{GS}, I_{D} = –250 μA</td>
<td>–0.4</td>
<td>–0.6</td>
<td>–1.5</td>
<td>V</td>
</tr>
<tr>
<td>∆V_{GS(th)}</td>
<td>Gate Threshold Voltage Temperature Coefficient</td>
<td>I_{D} = –250 μA, Referenced to 25°C</td>
<td>6.7</td>
<td>8.5</td>
<td></td>
<td>mV/°C</td>
</tr>
<tr>
<td>R_{DS(on)}</td>
<td>Static Drain–Source On–Resistance</td>
<td>V_{GS} = –4.5 V, I_{D} = –13.5 A</td>
<td>8.0</td>
<td>10.5</td>
<td></td>
<td>mΩ</td>
</tr>
<tr>
<td> </td>
<td> </td>
<td>V_{GS} = –2.5 V, I_{D} = –12 A</td>
<td>9.8</td>
<td>14</td>
<td></td>
<td></td>
</tr>
<tr>
<td> </td>
<td> </td>
<td>V_{GS} = –1.8 V, I_{D} = –10.5 A</td>
<td>9.0</td>
<td>13</td>
<td></td>
<td></td>
</tr>
<tr>
<td> </td>
<td> </td>
<td>V_{GS} = –4.5 V, I_{D} = –13.5 A, T_{J} = 125°C</td>
<td>6.7</td>
<td>8.5</td>
<td></td>
<td>mΩ</td>
</tr>
<tr>
<td>I_{D(on)}</td>
<td>On–State Drain Current</td>
<td>V_{GS} = –4.5 V, V_{DS} = –5 V</td>
<td>–50</td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>g_{FS}</td>
<td>Forward Transconductance</td>
<td>V_{DS} = –5 V, I_{D} = –13.5 A</td>
<td>70</td>
<td></td>
<td></td>
<td>S</td>
</tr>
<tr>
<td>Dynamic Characteristics</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ciss</td>
<td>Input Capacitance</td>
<td>V_{DS} = –10 V, V_{GS} = 0 V</td>
<td>8237</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Coss</td>
<td>Output Capacitance</td>
<td>I = 1.0 MHz</td>
<td>1497</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Crss</td>
<td>Reverse Transfer Capacitance</td>
<td></td>
<td>750</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Switching Characteristics (Note 2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_{on}</td>
<td>Turn–On Delay Time</td>
<td>V_{DD} = –10 V, I_{D} = –1 A</td>
<td>20</td>
<td>36</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{r}</td>
<td>Turn–On Rise Time</td>
<td>V_{GS} = –4.5 V, R_{GEN} = 6 Ω</td>
<td>24</td>
<td>38</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{off}</td>
<td>Turn–Off Delay Time</td>
<td>V_{DS} = –10 V, I_{D} = –13.5 A</td>
<td>300</td>
<td>480</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tf</td>
<td>Turn–Off Fall Time</td>
<td>V_{GS} = –4.5 V, I_{D} = 0 A</td>
<td>140</td>
<td>224</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Q_{g}</td>
<td>Total Gate Charge</td>
<td>V_{DS} = –10 V, I_{D} = –13.5 A</td>
<td>86</td>
<td>120</td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>Q_{gs}</td>
<td>Gate–Source Charge</td>
<td>V_{GS} = –4.5 V</td>
<td>20</td>
<td></td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>Q_{gd}</td>
<td>Gate–Drain Charge</td>
<td>V_{DS} = –10 V, I_{D} = –13.5 A</td>
<td>11</td>
<td></td>
<td></td>
<td>nC</td>
</tr>
</tbody>
</table>

## Drain–Source Diode Characteristics and Maximum Ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_{D}</td>
<td>Maximum Continuous Drain–Source Diode Forward Current</td>
<td>V_{GS} = 0 V, I_{D} = –2.1 A (Note 2)</td>
<td>–2.1</td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>V_{FSD}</td>
<td>Drain–Source Diode Forward Voltage</td>
<td>V_{GS} = 0 V, I_{S} = –2.1 A</td>
<td>–0.6</td>
<td>–1.2</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

Notes:

1. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

![Thermal Resistance Diagram]

Scale 1 : 1 on letter size paper
**Typical Characteristics**

**Figure 1.** On-Region Characteristics.

**Figure 2.** On-Resistance Variation with Drain Current and Gate Voltage.

**Figure 3.** On-Resistance Variation with Temperature.

**Figure 4.** On-Resistance Variation with Gate-to-Source Voltage.

**Figure 5.** Transfer Characteristics.

**Figure 6.** Body Diode Forward Voltage Variation with Source Current and Temperature.
Typical Characteristics

![Graph showing Gate Charge Characteristics](image1)

**Figure 7. Gate Charge Characteristics.**

![Graph showing Capacitance Characteristics](image2)

**Figure 8. Capacitance Characteristics.**

![Graph showing Maximum Safe Operating Area](image3)

**Figure 9. Maximum Safe Operating Area.**

![Graph showing Single Pulse Maximum Power Dissipation](image4)

**Figure 10. Single Pulse Maximum Power Dissipation.**

![Graph showing Transient Thermal Response Curve](image5)

**Figure 11. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.
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<th>ActiveArray™</th>
<th>FACT™</th>
<th>ImpliedDisconnect™</th>
<th>PACMAN™</th>
<th>SPM™</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bottomless™</td>
<td>FAST®</td>
<td>LittleFET™</td>
<td>Power247™</td>
<td>Stealth™</td>
</tr>
<tr>
<td>CoolFET™</td>
<td>FASTr™</td>
<td>MicroFET™</td>
<td>PowerTrench®</td>
<td>SuperSOT™-3</td>
</tr>
<tr>
<td>CROSSVOLT™</td>
<td>FRFET™</td>
<td>MicroPak™</td>
<td>QFET™</td>
<td>SuperSOT™-6</td>
</tr>
<tr>
<td>DOME™</td>
<td>GlobalOptoisolator™</td>
<td>MICROWIRE™</td>
<td>QS™</td>
<td>SuperSOT™-8</td>
</tr>
<tr>
<td>EcoSPARK™</td>
<td>GTO™</td>
<td>MSX™</td>
<td>QT Optoelectronics™</td>
<td>SyncFET™</td>
</tr>
<tr>
<td>EnSigna™</td>
<td>HiSeC™</td>
<td>MSXPro™</td>
<td>Quiet Series™</td>
<td>TinyLogic®</td>
</tr>
<tr>
<td>Programmable Active Droop™</td>
<td>OCX™</td>
<td>OPTOLOGIC®</td>
<td>RapidConfigure™</td>
<td>UHC™</td>
</tr>
<tr>
<td>Across the board, Around the world™</td>
<td>OCXPro™</td>
<td>OPTOPLANAR™</td>
<td>RapidConnect™</td>
<td>UltraFET®</td>
</tr>
<tr>
<td>The Power Franchise™</td>
<td>OCX™</td>
<td>SILENT SWITCHER®</td>
<td>SMART START™</td>
<td></td>
</tr>
</tbody>
</table>

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

<table>
<thead>
<tr>
<th>Datasheet Identification</th>
<th>Product Status</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Advance Information</td>
<td>Formative or In Design</td>
<td>This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.</td>
</tr>
<tr>
<td>Preliminary</td>
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</tr>
<tr>
<td>No Identification Needed</td>
<td>Full Production</td>
<td>This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.</td>
</tr>
<tr>
<td>Obsolete</td>
<td>Not In Production</td>
<td>This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.</td>
</tr>
</tbody>
</table>