



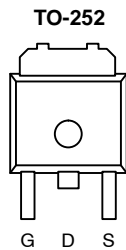
# N-Channel 60-V (D-S), 175°C MOSFET, Logic Level



PRODUCT SUMMARY		
V <sub>DS</sub> (V)	r <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>a</sup>
60	0.022 @ V <sub>GS</sub> = 10 V	30
	0.025 @ V <sub>GS</sub> = 4.5 V	30

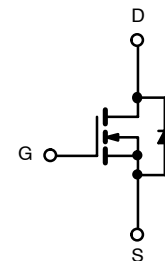
### FEATURES

- TrenchFET® Power MOSFET
- 175°C Maximum Junction Temperature
- 100% R<sub>g</sub> Tested



Top View

Drain Connected to Tab



N-Channel MOSFET

Ordering Information: SUD40N06-25L  
 SUD40N06-25L—E3 (Lead (Pb)-Free)

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25°C UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Unit
Gate-Source Voltage		V <sub>GS</sub>	± 20	V
Continuous Drain Current (T <sub>J</sub> = 175°C) <sup>b</sup>	T <sub>C</sub> = 25°C	I <sub>D</sub>	30	A
	T <sub>C</sub> = 100°C		30	
Pulsed Drain Current		I <sub>DM</sub>	100	
Continuous Source Current (Diode Conduction)		I <sub>S</sub>	34	
Avalanche Current		I <sub>AR</sub>	34	
Repetitive Avalanche Energy (Duty Cycle ≤ 1%)		L = 0.1 mH E <sub>AR</sub>	58	mJ
Maximum Power Dissipation	T <sub>C</sub> = 25°C	P <sub>D</sub>	75	W
	T <sub>A</sub> = 25°C		1.4 <sup>b</sup> , 2.5 <sup>c</sup>	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to 175	°C

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Limit	Unit
Maximum Junction-to-Ambient	Free Air, FR4 Board Mount	R <sub>thJA</sub>	60	°C/W
	Free Air, Vertical Mount		110	
Maximum Junction-to-Case		R <sub>thJC</sub>	2.0	

Notes:

- a. Package limited.
- b. Free air, vertical mount.
- c. Surface mounted on 1" x 1" FR4 Board, t ≤ 10 sec.

For SPICE model information via the Worldwide Web: <http://www.vishay.com/www/product/spice.htm>



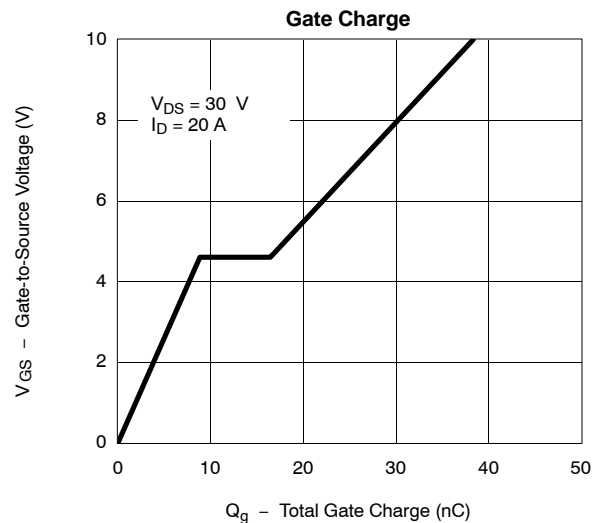
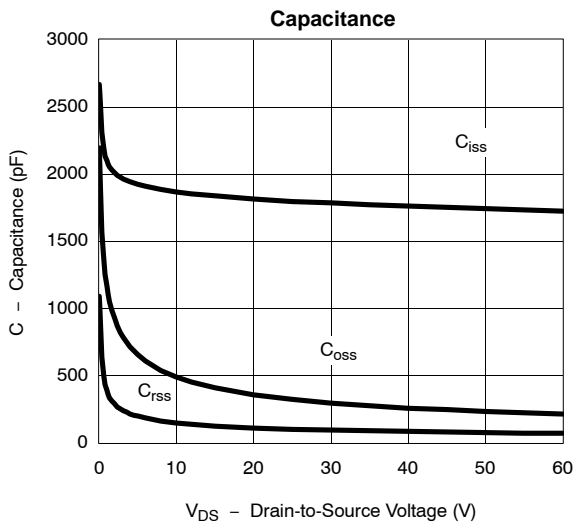
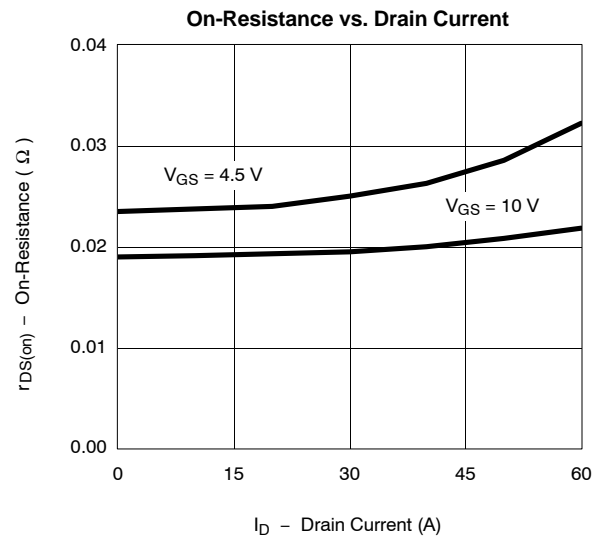
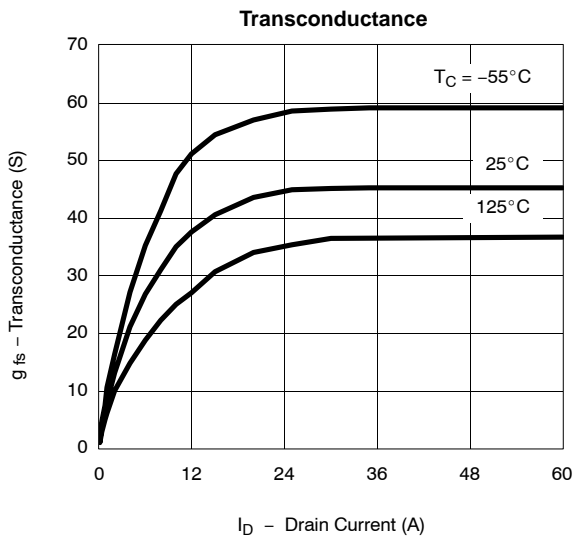
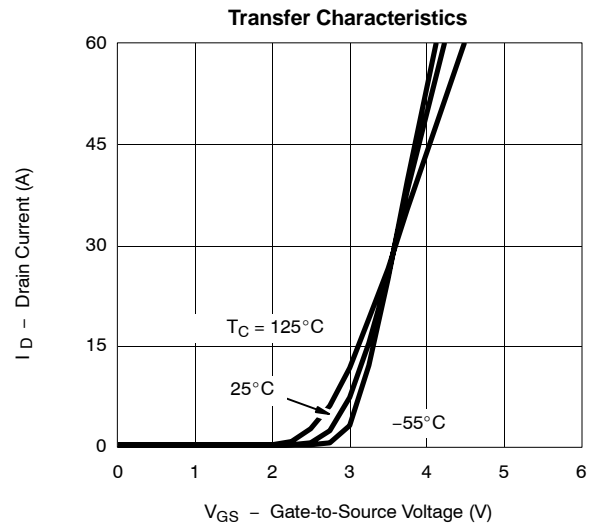
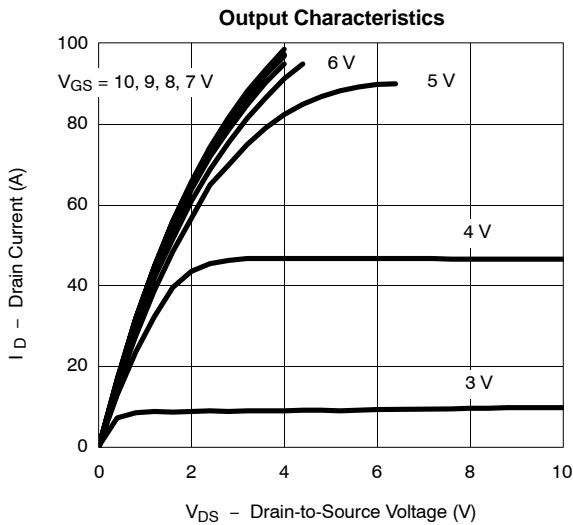
SPECIFICATIONS (T <sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ <sup>a</sup>	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	60			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.0	2.0	3.0	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C			50	
		V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 175 °C			150	
On-State Drain Current <sup>b</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 10 V	20			A
Drain-Source On-State Resistance <sup>b</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A			0.022	Ω
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A, T <sub>J</sub> = 125 °C			0.043	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A, T <sub>J</sub> = 175 °C			0.053	
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 20 A			0.025	
Forward Transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 20 A				S
<b>Dynamic</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1 MHz		1800		pF
Output Capacitance	C <sub>oss</sub>			350		
Reverse Transfer Capacitance	C <sub>rss</sub>			100		
Total Gate Charge <sup>c</sup>	Q <sub>g</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 40 A		40	60	nC
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>			9		
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			10		
Gate Resistance	R <sub>g</sub>		1		3.5	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 30 V, R <sub>L</sub> = 0.9 Ω I <sub>D</sub> = 20 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 2.5 Ω		10	20	ns
Rise Time <sup>c</sup>	t <sub>r</sub>			9	20	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			28	50	
Fall Time <sup>c</sup>	t <sub>f</sub>			7	15	
<b>Source-Drain Diode Ratings and Characteristics (T<sub>C</sub> = 25 °C)</b>						
Pulsed Current	I <sub>SM</sub>				20	A
Diode Forward Voltage	V <sub>SD</sub>	I <sub>F</sub> = 20 A, V <sub>GS</sub> = 0 V		1.0	1.5	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 20 A, di/dt = 100 A/μs		48	100	ns

## Notes:

- For design aid only; not subject to production testing.
- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- Independent of operating temperature.

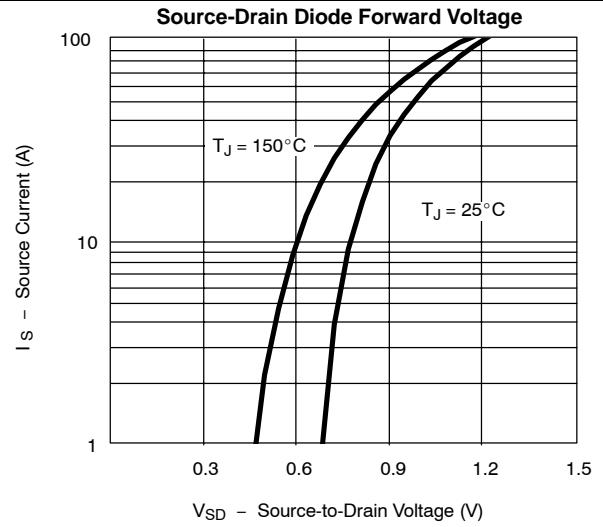
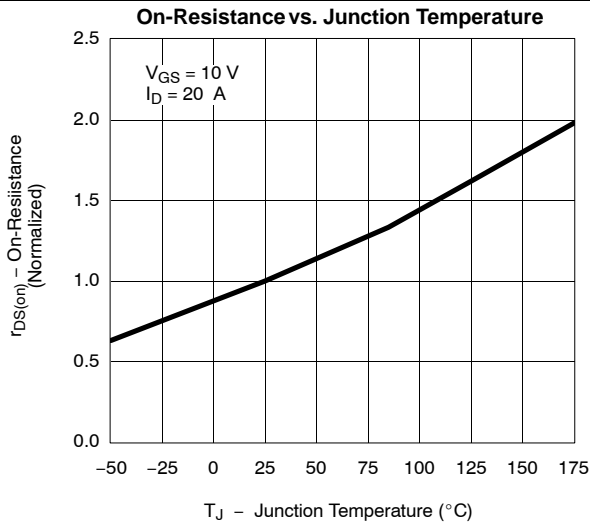
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**





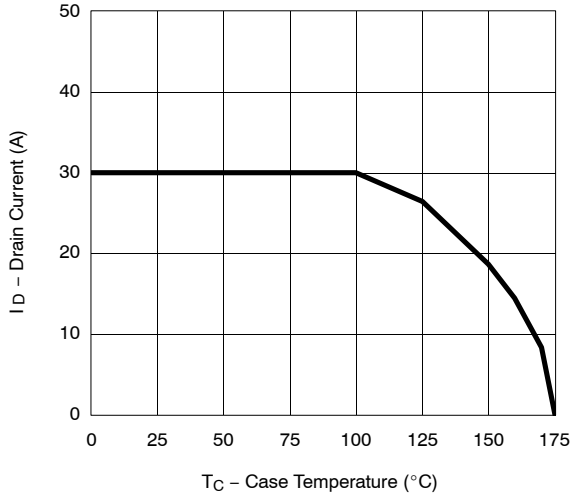
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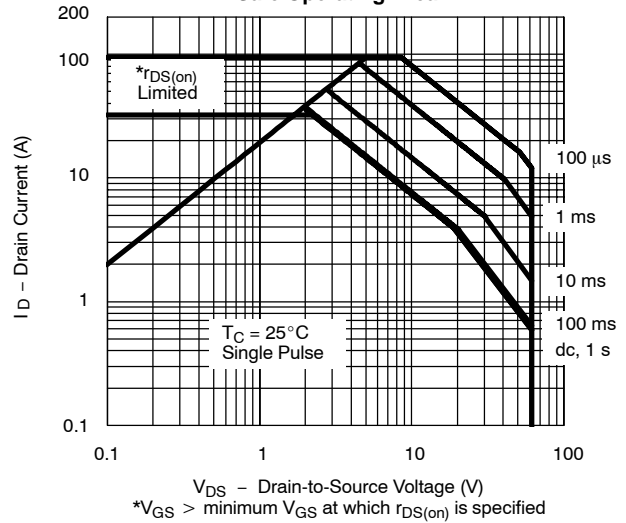


**THERMAL RATINGS**

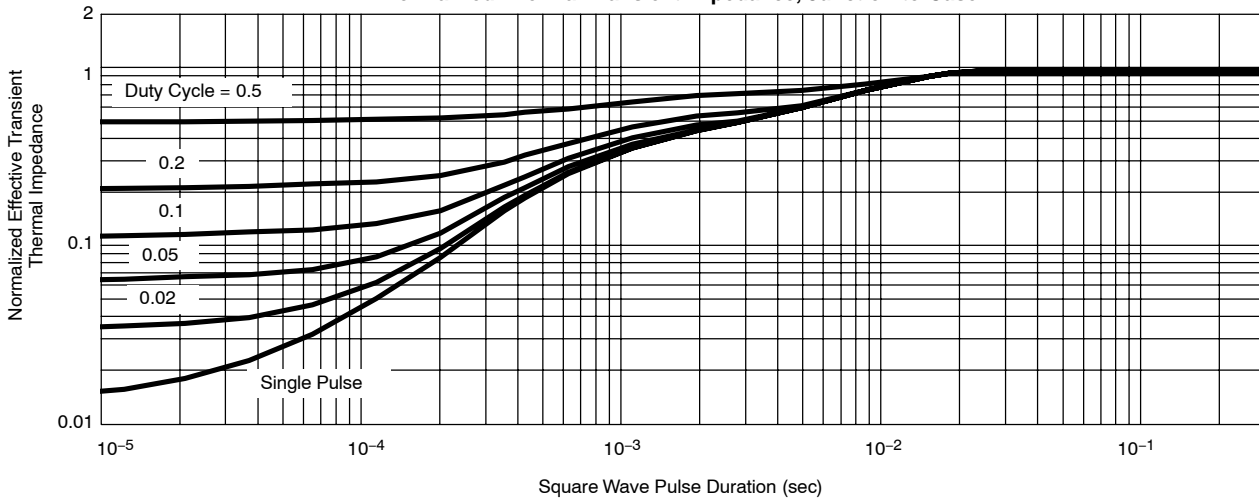
**Drain Current vs. Case Temperature**



**Safe Operating Area**



**Normalized Thermal Transient Impedance, Junction-to-Case**



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